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# Applying 6 Sigma in Quality Improvement of TFT-LCD Panel

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**Abstract**

Product quality and manufacturing cost are crucial to winning for TFT-LCD manufacturers facing a very competitive global market due to prosperous development of information technology. TFT-LCD panel manufacturers therefore are going all out in the pursuit of continuous cost reduction and upgraded product quality. Many of them have introduced in the 6 sigma management methodology that creates high profitability in the hope to upgrade product quality and yield so to further reduce wastes of cost and nonconformities. Whereas manufacturers are not necessarily aware of the key quality process to be improved in the promotion of the 6 sigma methodology, this study attempts to analyze the Characteristic of critical-to-quality (CTQ) of the TFT-LCD panel manufacturing process and to locate the critical process on top priority pending improvement for serving an entry using the Multi-Characteristic Product Capability Analysis Chart (MPCAC). Therefore, improvement efficiency and chance of success in promotion of the 6 sigma method will be increased for TFT-LCD panel manufacturers making the best out of the methodology recommended by the study.

*Keywords:* 6 Sigma; Critical to Quality; TFT-LCD Panel; Multi-Characteristic Product Capability Analysis Chart

## 1. Introduction

The display is a vital media for man-machine communication. In the past, the Cathode Ray Tube (CRT) dominated; however, as electronic technology continues to advance and the emergence of communication, IA, and multi-media markets, continuous development of diversified display technologies has gradually exited and taken the place of the CRT display. TFT-LCD (Thin Film Transistor Liquid Crystal Display) is penetrating into human daily life by day. In addition to providing better visual enjoyment for viewers in the performance of stable colors and images without glittering, TFT-LCD delivers other advantages of being compact, low radiation, and low power consumption for people while enjoying video, entertainment, and information without exposing their health to hazards.

While the product life cycle of the panel industry in Taiwan is approaching its mature phase and manufacturers are putting into production using newer generation technology, over supply situation is predicted when the production capacity reaches its commercial scale and the expansion continues, plus the fierce competition from Japan and South Korea. Moreover, it may appear compact, a TFT-LCD panel actually an assembly of more than twenty items of parts and materials is essentially comprised of Color

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Filter (CF), Driver IC Polarizer, Glass Substrate, Backlight Module, and other materials with a total cost of materials consuming 65% or more as of the grand total cost. Wherein, color filter, driver IC, glass substrate, and polarizer are key components to the TFT-LCD industry today. However, the production of TFT-LCD involves highly complicated process. The process includes many chemical materials and thin glass substrates; and any variance in quality may prevent many in-process items from being reworked thus to affect the subsequent assembly of module and/or the function expected from the finished product. Eventually, cost waste is unavoidable; therefore, improved process capability and quality will minimize waste in production cost.

The manufacturing process of TFT-LCD may break into three key workstations, respectively, the process of substrate array and that of the color filter in the upper stream; the process of crystal panel assembly (Cell) in the mid stream; and module erection in the lower stream. Wherein, the array process in the upper stream is one of the most important processes in the production of TFT-LCD panel. Similar to the process of manufacturing semiconductor, the array process starts with rinsing the non-alkali glass substrate before entering into a thin film process for multiple layers including five layers of mask process, respectively gate electrode, semiconductor, transparent conduction, source electrode, and source/drain metal, and protection film to go through the procedure of photo-resist, exposure, development, etching, and photo-resist stripping in sequence to stack up by layer circuits and devices needed to form an array substrate of the thin film transistor (TFT). Whereas devices and connection wires are comparatively minute in a semiconductor, function of circuit in the chip is vulnerable to be damaged by any quality variance including inconsistent application of photo-resist, incorrect location of the pattern for exposure, and the etching wire being too wide or narrow occurred during the process; and the circuit shortage or broken further leads to failure of the IC, which in turn compromises the middle and the final flow paths of the process or flaws to the function of the product, and wastes of cost. Therefore, this paper focuses its discussion on the flow path of array in the process characterized by whether the thickness of the photo resist applied is uniform, if the pattern exposed is correctly located; and whether the width of the etching wire is proper.

According to [1-3], the product will be only accepted when each quality requirement is met. However, so far the quality evaluation for the array process of the TFT-LCD panel is not complete. Some experts evaluate only the entire TFT-LCD process without providing a set of improvement method and mode specifically for the array process. This paper attempts to set forth a quality evaluation mode for the array substrate process based on those five mask processes and three CTQ characteristics as described above to evaluate or measure if these processes have met quality requirements. TFT-LCD panel manufacturers upon promoting the 6 Sigma DMAIC flow path improvement mode sometimes are not sure about the CTQ Characteristic to be improved. With the evaluation mode developed by this paper, manufacturers are able to objectively locate CTQ Characteristic and make the improvements, and to have better chances for successful promotion of the 6 Sigma method.

## 2. TFT-LCD Panel Quality Evaluation Mode

As described above, the array process, similar to that for the semiconductor, has to go through five courses of mask process with each mask process comprised of coating of photo-resist, exposure, development, and etching steps. Whereas all three CTQ Characteristic are symmetrical and of Nominal-the-Best, Boyles [4]

proposed $C_{pk}$, a process capability index of Nominal-the-Best for process analysis. However, though the index $C_{pk}$ guarantees a certain range of yield for the process, it fails to indicate the actual value of the process yield. Therefore, Boyles [5] has defined $S_{pk}$, a new index of one-on-one mathematic relation for the process yield. This paper will use the index of $S_{pk}$ for evaluation of the process capability of each key process quality Characteristic of TFT-LCD panel defined as follows:

$$S_{pkij} = \frac{1}{3}\Phi^{-1}\left\{\frac{1}{2}\Phi\left(\frac{USL_{ij}-\mu_{ij}}{\sigma_{ij}}\right)+\frac{1}{2}\Phi\left(\frac{\mu_{ij}-LSL_{ij}}{\sigma_{ij}}\right)\right\} \tag{1}$$

Wherein $i$ represents the $i^{th}$ mask process; $i$ = 1,…,5 ,$j$, the $j^{th}$ CTQ Characteristic process; $j$ = 1, 2, 3; $\Phi$ ; the accumulated opportunity function of standard normal distribution; and $\Phi^{-1}$, the inverse function of $\Phi$. In fact, there is the one-on-one mathematic relation among the $S_{pkij}$ process yields; therefore, the index of $S_{pkij}$ radio is an index of $C_{pk}$ that better reflects the process yield. Obviously, if $S_{pkij} = C$, then:

$$P_{ij} = 2 - 2\Phi(3C) \tag{2}$$

Wherein, $P_{ij}$ represents the rejection rate of the $j^{th}$ CTQ Characteristic process of the $i^{th}$ mask process. Steps in the entire TFT-LCD panel process are inter-dependent on one another, and any quality variance in the front section of the process may affect the quality of the subsequent steps; therefore, the relationship between the product rejection rate of the product of TFT-LCD panel and three key process qualities Characteristic is expressed as follows:

$$\text{Max}\left\{P_{i1},...,P_{i3}\right\} \le p_i \le \sum_{j=1}^{3} P_{ij} \tag{3}$$

According to eq. (3), it appears that $P_{ij} = 2 - 2\Phi(3S_{pkij})$ ; thus, the relationship between the product rejection rate, $P_{ij}$ of each mask process for the TFT-LCD panel and the process capability index, $S_{pkij}$ is expressed as follows:

$$P_i \le \sum_{j=1}^{3} P_{ij} = \sum_{j=1}^{3}\left[2 - 2\Phi\left(3S_{pkij}\right)\right] \tag{4}$$

According to those equations given above, this paper by following the method disclosed by Chen et al. (2003) to define a process quality index that is capable of reflecting the rejection rate of the mask process as follows:

$$C_{T_i} = \frac{1}{3}\Phi^{-1}\left\{1-\sum_{j=1}^{3}\left[1-\Phi\left(3S_{pkij}\right)\right]\right\} \tag{5}$$

According to equation (5), both sides of the equation are multiplied by (3), $\Phi$ and transposition compiled to solve a relationship equation between the rejection rate of mask process and the index $C_{T_i}$ as follows:

$$P_i = 2 - 2\Phi\left(3C_{T_i}\right) \tag{6}$$

When the value of $C_{T_i}$ i.e., the process capability index of LCD panel mask process is greater, the

rejection rate, ($P_j$), of each CTQ Characteristic process tends to get lower. Should P represent the process rejection rate of the entire substrate array process, the rejection rate of the entire substrate array process is expressed as follows since the steps of the entire TFT-LCD panel process are interdependent:

$$P = \sum_{i=1}^{5} P_i \tag{7}$$

Whereas $P_i = 2 - 2\Phi\left(3C_{T_i}\right)$, the rejection rate of the entire process of substrate array may be expressed as follows:

$$P = \sum_{i=1}^{5} P_i = \sum_{i=1}^{5}\left[2 - 2\Phi\left(3C_{T_i}\right)\right] \tag{8}$$

According to those equations give above, this paper defines $C_T$, a total index of process capability that reflects the rejection rate of the entire substrate array process as follows:

$$C_T = \frac{1}{3}\Phi^{-1}\left\{1 - \sum_{i=1}^{5}\left[1 - \Phi\left(3C_{T_i}\right)\right]\right\} \tag{9}$$

Then equation (5) of the definition of $C_{Ti}$ substitutes the definition given in equation of $C_T$ (9), $C_T$ is redefined as follows:

$$C_T = \left(\frac{1}{3}\right)\Phi^{-1}\left\{1 - \sum_{i=1}^{5}\left[1 - \Phi\left(\left(\sum_{j=1}^{3}\left(2 - 2\Phi\left(3S_{pkij}\right)\right)\right)\right)\right]\right\} \tag{10}$$

Both sides of eq. (10) are multiplied by 3, $\Phi$, transposed, and substituted by eq. (9) or alternatively, both sides of eq. (11) are multiplied by 3, $\Phi$, transposed, and substituted by eq. (4) and eq. (9) to solve an equation of relationship between the rejection rate of the entire array substrate process and the index $C_T$ as follows:

$$P = 2 - 2\Phi(3C_T) \tag{11}$$

It appears that when the value of the index $C_T$ of the entire array substrate process is greater, the rejection rate ($P$) of each mask process gets lower.

## 3. Process Capability Analysis Chart Determination of CTQ Characteristic Process Capability Index Values of the $i^{th}$ Mask Process and the Mask Process

Whereas there are five different mask processes in the array substrate process and each mask process contains three CTQ Characteristic processes, the value of the index of each mask process must be higher than that of the entire array substrate process (higher quality) so to meet the level of the entire array substrate process quality index demanded by the customer according to perspectives [3, 6-7]. Assume that the demanded value of product quality index of the entire array substrate process is $C_T = u$, i.e.,

$$C_T = \frac{1}{3}\Phi^{-1}\left\{1 - \sum_{i=1}^{5}\left[1 - \Phi\left(3C_{T_i}\right)\right]\right\} = u \tag{12}$$

If it is demanded that, $v$, the value of the process capability index of each mask process is the same, the value of $w$ can be inferred from eq. (12) as follows:

$$\frac{1}{3}\Phi^{-1}\left\{1-\sum_{i=1}^{5}\left[1-\Phi\left(3v\right)\right]\right\}=u \Rightarrow \quad v=\frac{1}{3}\Phi^{-1}\left[\frac{\Phi\left(3u+4\right)}{5}\right] \tag{13}$$

Since each mask process of the entire array substrate process includes several CTQ Characteristic processes, the value of the index of each CTQ Characteristic process must be greater than that of the mask process so to meet the level as demanded by the customer. When the value of the process capability index of each mask process in the entire array substrate process is demanded as expressed in $C_{T_i}=v$, i.e.,

$$C_{T_i}=\frac{1}{3}\Phi^{-1}\left\{1-\sum_{j=1}^{3}\left[1-\Phi\left(3S_{pkij}\right)\right]\right\}=v \tag{14}$$

When it is demanded that the value of CTQ process capability index of each mask process is the same *w*, the value of *w* is inferred according to eq. (14) as follows:

$$C_{T_i}=\frac{1}{3}\Phi^{-1}\left\{1-\sum_{j=1}^{3}\left[1-\Phi\left(3w\right)\right]\right\}=v \Rightarrow \quad w=\frac{1}{3}\Phi^{-1}\left[\frac{\Phi\left(3v+4\right)}{3}\right] \tag{15}$$

For example, if ($C_T$), the value of process capability index of the TFT-LCD panel array process is demanded to reach the quality level of 1, it is solved by operating eq. (15) that the value of the process capability index ($C_{T_i}$) must attain 1.15 or higher for assurance of the process quality level of the product. Furthermore, when the process capability of each mask process is demanded to reach a quality level of 1.152, the eq. (13) is operated to reduce that the value of the CTQ Characteristic process capability index ($C_{T_{ij}}$) must attain 1.248 to assure of attaining the quality objective of the entire array process.

## 4. Applying MPCAC CTQ in Definition of 6 Sigma Improvement Method

According to [8], the concept of the 6 Sigma was initially proposed by Motorola in 1987 and that paid Motorola the winner of the Malcom Baldrige National Quality Award. In a DMAIC flow path of the 6 Sigma proposed by [9], it is argued that the definition of issue must be specific. Sometimes a manufacturer in promoting quality improvement using the 6 Sigma is not necessarily having exact understanding of the CTQ; it is a must to develop objective methodology in locating the CTQ process for serving a specific entry for TFT-LCD panel makers in pushing forward the 6-Sizma for quality improvement to achieve more significant results in upgrading product quality.

Whereas this paper has delivered a complete introduction of CTQ characteristics and the process capability index, $S_{pkij}$ to serve as a tool in the evaluation of the Array process quality in each mask process of the entire array substrate process in the previous section, this paper based on the introduction further develops a set of measurement mode followed with detailed analysis to realize through measurement whether each mask process and CTQ characteristic process capabilities of the entire array process, and performance analysis to the process found defective for providing improvement project e depending on the results of analysis. Whereas each mask process of the array substrate process contains three CTQ

characteristics and the specification of each CTQ characteristic is of Nominal-the-Best and symmetric allowance, this paper by referring to the method proposed by Chen et al. [3] has $\delta = (\mu - T)/d$ as the x-coordinate and $\gamma = \sigma/d$ as the y-coordinate in developing a Multi-Characteristic Product Capability Analysis Chart-MPCAC/$S_{pk}$ that is capable of evaluating the array process; accordingly the index of $S_{pk}$ is expressed in a function of ($\delta$, $\gamma$) as follows:

$$S_{pk} = \frac{1}{3}\Phi^{-1}\left\{\frac{1}{2}\Phi\left(\frac{1-\delta}{\gamma}\right)+\frac{1}{2}\Phi\left(\frac{1+\delta}{\gamma}\right)\right\} \tag{16}$$

It appears that when $\mu = LSL$, $\delta = -1$; when $\mu = USL$, $\delta = 1$; and when $\mu = T$, $\delta = 0$. Accordingly, we may solve the value of the process capability index corresponding to the process control grade based on the numbers of the mask process and CTQ characteristic of the array substrate process as described earlier in this paper. According to [10], Motorola's 6 Sigma quality level is referred to when the process criteria $\sigma = d/6$ with an allowed process deviation of $1.5\sigma$. Under the circumstances, the value of $S_{pk}$ corresponding to the 6 Sigma should be greater than 1.55. Since the entire TFT-Array process is comprised of five courses of critical mask process with each further contains three CTQ characteristics, both eq. (13) and eq. (15) are reduced to solve that the lower limits of the corresponding CTQ mask process index $S_{pki}$ and the CTQ characteristic index $S_{pkij}$ are respectively $S_{pki}$=1.657 and $S_{pkij}$=1.727. Similarly, the same method is used to respectively solve values of $S_{pki}$ and $S_{pkij}$ corresponding to the quality levels of 5 Sigma, 4 Sigma, and 3 Sigma as shown in Table 1.

Based on values of $S_{pki}$ and $S_{pkij}$ corresponding to each quality level as listed in Table 1, a contour map for each value of $S_{pk}$ is plotted according to eq. (16) thus to form the Multi-Characteristic Product Capability Analysis Chart-MPCAC/$S_{pk}$ as illustrated in Fig. 1. Subsequently, by following to the concepts of $\overline{X} - S$ Control Map with the optimal condition taking place when the number of samples n > 10, this paper has the sample size, n=11 for each unit making a total of thirty units, m=30 in the stabilized process for respectively solving $\overline{\overline{X}}$ and $\overline{S}$ to serve estimation parameters of $\delta$ and $\gamma$. Accordingly, in this paper, $\delta$ is related to X- coordinate; and $\gamma$, Y-coordinate with equations to estimate $\delta$ and $\gamma$ expressed as follows:

$$\hat{\delta} = \frac{\overline{\overline{X}}_j - T_j}{d_j} \tag{17}$$

$$\hat{\gamma} = \frac{\overline{S_j}}{d_j} \tag{18}$$

In this real case, the manufacturing process for the TFT-LCD panel may be divided into the pre-cell process (array process) and panel assembly process (cell process). The array process includes three CTQ Characteristics: (1) photo-resist coating thickness, (2) location of pattern, and (3) etching wire width. These entire Characteristic are of Nominal-the-Best and in symmetrical specification as listed in Table 2.

Table 1 Array Substrate Process Index Value Corresponding to Quality Level

| Quality Level | Array Substrate Process (u) | Mask Process (v) | CTQ Characteristics (w) |
|---|---|---|---|
| 6 sigma | 1.550000 | 1.657215 | 1.726834 |
| 5 sigma | 1.230000 | 1.360319 | 1.443140 |
| 4 sigma | 0.910000 | 1.074474 | 1.175262 |
| 3 sigma | 0.610000 | 0.823876 | 0.947329 |

Table 2 Index Value & Coordinates Data of CTQ Characteristic by Mask Process

| Mask Process | CTQ Characteristic | Code | *Target* | $\hat{\delta}$ | $\hat{\gamma}$ |
|---|---|---|---|---|---|
| Metal Layer of Gate Electrode (A) | 1. Coating of Photo Resist | $A_1$ | 3000 | -0.59 | 0.27 |
| | 2. Exposure | $A_2$ | 3 | -0.02 | 0.19 |
| | 3. Etching | $A_3$ | 12 | 0.19 | 0.27 |
| Continuous Film Coasting Process of Semiconductor (B) | 1. Coating of Photo Resist | $B_1$ | 1750 | -0.52 | 0.23 |
| | 2. Exposure | $B_2$ | 3 | -0.06 | 0.22 |
| | 3. Etching | $B_3$ | 12 | 0.33 | 0.27 |
| Transparent Conduction Layer (C) | 1. Coating of Photo Resist | $C_1$ | 500 | -0.34 | 0.24 |
| | 2. Exposure | $C_2$ | 3 | -0.01 | 0.23 |
| | 3. Etching | $C_3$ | 5.3 | 0.28 | 0.29 |
| Source Electrode/Drain Metal Layer Process (D) | 1. Coating of Photo Resist | $D_1$ | 2000 | -0.21 | 0.32 |
| | 2. Exposure | $D_2$ | 3 | -0.17 | 0.18 |
| | 3. Etching | $D_3$ | 5.3 | 0.33 | 0.24 |
| Protection Film Process (E) | 1. Coating of Photo Resist | $E_1$ | 400 | -0.21 | 0.28 |
| | 2. Exposure | $E_2$ | 3 | 0.05 | 0.22 |
| | 3. Etching | $E_3$ | 10 | 0.02 | 0.27 |

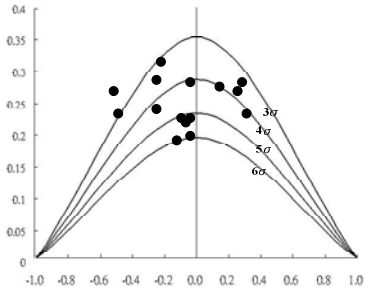


Fig. 1 Multi- Characteristic Product Capability Analysis Chart (MPCAC)

As described above, judging from each CTQ characteristic process coordinates as illustrated in Fig. 1, the exposure process in each mask process has reached the quality level of 4 Sigma; wherein, the exposure process for the source/drain metal layer is found with the best performance to reach quality level of 5 Sigma while the etching process in each mask process has reached the quality level of 3 Sigma. Finally, in the process of coating of photo-resist, the quality level of each mask process falls between edges of 3 Sigma, wherein, the lowest quality level is found with the photo-resist coating process for the gate

electrode metal layer, significantly showing insufficiency either in precision or accuracy of the process. Therefore, upon promoting the 6 Sigma for quality improvement by TFT-LCD manufacturers, the photo-resist coating process for the gate electrode metal layer shall be put on the top priority pending improvement.

## 5. Summary

TFT-LCD tends to exit the conventional monitor thanks to ever advancing in the flat display technology and emergence of the multi-media market; however, in facing the coming of the era of digital technology and wideband, the demand on TFT-LCD will see a significant growth. Therefore, leading panel manufacturers at home and overseas are making inputs of massive capitals to build plants for production, leading the TFT-LCD industry in Taiwan to become a key town of global production after that for mother boards and displays. To upgrade product competition strength, many manufacturers have introduced the 6 Sigma quality improvement method to raise product quality and yield thus to reduce wastes of cost. Upon promoting the 6 Sigma method, manufacturers sometimes have to face the fact that they are not very sure of which CTQ process that warrants improvement and the ignorance may well compromise the results of improvement. Accordingly, this paper first attempts to locate the CTQ characteristics of the process of TFT-LCD panel before borrowing the method proposed by Chen et al. [3] to develop a quality evaluation mode for the TFT-LCD panel according to the process capability index ($S_{pk}$) proposed by Boyles [5] and to further develop Multi- Characteristic Product Capability Analysis Chart (MPCAC) based on the 6 Sigma as perceived; later, values of process capability indices of all CTQ characteristic processes are plotted on the analysis chart for us to locate the quality level for each CTQ characteristic process and to learn the precision and accuracy of the process based on where each CTQ characteristic is located on the chart for further analysis in identifying the critical process that should be put on the top priority pending improvement to serve as an entry in the promotion of the 6 Sigma thus to have the optimal results for TFT-LCD panel manufacturers resolved to the 6 Sigma quality improvement project.

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