

重新查詢

友善列印

0971學期 課程基本資料

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|---------|----------|---------|-----------------------------|
| 系所 / 年級 | 資工系 2年級 | 課號 / 班別 | 64U00084 / B |
| 學分數 | 3學分 | 選 / 必修 | 必修 |
| 科目中文名稱 | 數位系統邏輯設計 | 科目英文名稱 | Digital system logic design |
| 主要授課老師 | 關國裕 | 開課期間 | 一學期 |
| 人數上限 | 58 人 | 已選人數 | 59人 |

起始週 / 結束週 / 上課地點 / 上課時間

第1週 / 第18週 / I309 / 星期2第05節
第1週 / 第18週 / I309 / 星期2第06節
第1週 / 第18週 / I309 / 星期2第07節

請各位同學遵守智慧財產權觀念；請勿非法影印。

教學綱要

- 一、教學目標(Objective) This course is aimed at introducing the fundamental concepts and the basic tools used in the logic design of digital systems.
- 二、先修科目(Pre Course)
- 三、教材內容(Outline)
- 四、教學方式(Teaching Method) 講授、研討、媒體運用、專題實作
- 五、參考書目(Reference) Logic and Computer Design Fundamentals, 3rd Edition M. Morris Mano & Charles R. Kime Pearson Prentice Hall (Ch1~7) Digital Design, 3rd Edition M. Morris Mano Prentice Hall. (Ch1~7)

| | | |
|-----------|--|-----|
| 2008/9/17 | Digital Computers and Information -Digital Computers -Number Systems -Arithmetic Operations -Decimal, Gray, and Alphanumeric Codes | 關國裕 |
| 2008/9/24 | Digital Computers and Information -Digital Computers -Number Systems -Arithmetic Operations -Decimal, Gray, and Alphanumeric Codes | 關國裕 |
| 2008/10/1 | Digital Computers and Information -Digital Computers -Number Systems -Arithmetic Operations -Decimal, Gray, and Alphanumeric Codes | 關國裕 |

六、教學進度(Syllabi)

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|------------|---|-----|
| 2008/10/8 | Digital Computers and Information -Digital Computers -Number Systems -Arithmetic Operations -Decimal, Gray, and Alphanumeric Codes | 關國裕 |
| 2008/10/15 | Boolean Algebra and Logic Gates -Binary Logic and Gates - Boolean Algebra | 關國裕 |
| 2008/10/22 | Boolean Algebra and Logic Gates -Binary Logic and Gates - Boolean Algebra | 關國裕 |
| 2008/10/29 | Gate-Level Minimization -Two-Level Circuit Optimization - Multiple-Level Circuit Optimization | 關國裕 |
| 2008/11/5 | Gate-Level Minimization -Two-Level Circuit Optimization - Multiple-Level Circuit Optimization | 關國裕 |
| 2008/11/12 | Team Project or Mid-term Exam | 關國裕 |
| 2008/11/19 | Combinational Logic -Combinational Logic Design Flow - Combinational Functions and Circuits | 關國裕 |
| 2008/11/26 | Combinational Logic -Combinational Logic Design Flow - Combinational Functions and Circuits | 關國裕 |
| 2008/12/3 | Combinational Logic -Combinational Logic Design Flow - Combinational Functions and Circuits | 關國裕 |
| 2008/12/10 | Combinational Logic -Combinational Logic Design Flow - Combinational Functions and Circuits | 關國裕 |
| 2008/12/17 | Synchronous Sequential Logic -Latches and Flip-Flops - Synchronous Sequential Circuit Analysis and Design Flow - Registers and Counters | 關國裕 |
| 2008/12/24 | Synchronous Sequential Logic -Latches and Flip-Flops - Synchronous Sequential Circuit Analysis and Design Flow - Registers and Counters | 關國裕 |
| 2008/12/31 | Synchronous Sequential Logic -Latches and Flip-Flops - Synchronous Sequential Circuit Analysis and Design Flow - Registers and Counters | 關國裕 |
| 2009/1/7 | Synchronous Sequential Logic -Latches and Flip-Flops - Synchronous Sequential Circuit Analysis and Design Flow - Registers and Counters | 關國裕 |
| 2009/1/14 | Team Project or Final Exam | 關國裕 |

七、評量方式(Evaluation)

Participation: 10% Team Project: 30% Mid-term Exam: 30% Final Exam: 30%

八、講義位址(http://)

九、教育目標

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