0971學期 課程基本資料

系所 / 年級	資工系 2年級	課號 / 班別	64U00084 / A
學分數	3學分	選 / 必修	必修
科目中文名稱	數位系統邏輯設計	科目英文名稱	Digital system logic design
主要授課老師	關國裕	開課期間	一學期
人數上限	60 人	已選人數	60人

起始週 / 結束週 / 上課地點 / 上課時間

第1週 / 第18週 / I527 / 星期3第02節
第1週 / 第18週 / I527 / 星期3第03節
第1週 / 第18週 / I527 / 星期3第04節

教學綱要

一、教學目標(Objective)	This course is aimed at introducing the fundamental concepts and the basic tools used in the logic design of digital systems.
二、先修科目(Pre Course)	
三、教材內容(Outline)	
四、教學方式(Teaching Method)	講授、研討、媒體運用、專題實作
五、參考書目(Reference)	Logic and Computer Design Fundamentals, 3rd EditionM. Morris Mano & Charles R. KimePearson Prentice Hall(Ch1~7) Digital Design, 3rd EditionM. Morris ManoPrentice Hall.(Ch1~7)

2008/9/18	Digital Computers and Information -Digital Computers -Number Systems -Arithmetic Operations -Decimal, Gray, and Alphanumeric Codes	關國裕
2008/9/25	Digital Computers and Information -Digital Computers -Number Systems -Arithmetic Operations -Decimal, Gray, and Alphanumeric Codes	關國裕
2008/10/2	Digital Computers and Information -Digital Computers -Number Systems -Arithmetic Operations -Decimal, Gray, and Alphanumeric Codes	關國裕

六、教學進度**(Syllabi)**	2008/10/9	Digital Computers and Information -Digital Computers -Number Systems -Arithmetic Operations -Decimal, Gray, and Alphanumeric Codes	關國裕
	2008/10/16	Boolean Algebra and Logic Gates -Binary Logic and Gates -Boolean Algebra	關國裕
	2008/10/23	Boolean Algebra and Logic Gates -Binary Logic and Gates -Boolean Algebra	關國裕
	2008/10/30	Gate-Level Minimization -Two-Level Circuit Optimization -Multiple-Level Circuit Optimization	關國裕
	2008/11/6	Gate-Level Minimization -Two-Level Circuit Optimization -Multiple-Level Circuit Optimization	關國裕
	2008/11/13	Team Project or Mid-term Exam	關國裕
	2008/11/20	Combinational Logic -Combinational Logic Design Flow -Combinational Functions and Circuits	關國裕
	2008/11/27	Combinational Logic -Combinational Logic Design Flow -Combinational Functions and Circuits	關國裕
	2008/12/4	Combinational Logic -Combinational Logic Design Flow -Combinational Functions and Circuits	關國裕
	2008/12/11	Combinational Logic -Combinational Logic Design Flow -Combinational Functions and Circuits	關國裕
	2008/12/18	Synchronous Sequential Logic -Latches and Flip-Flops -Synchronous Sequential Circuit Analysis and Design Flow -Registers and Counters	關國裕
	2008/12/25	Synchronous Sequential Logic -Latches and Flip-Flops -Synchronous Sequential Circuit Analysis and Design Flow -Registers and Counters	關國裕
	2009/1/1	Synchronous Sequential Logic -Latches and Flip-Flops -Synchronous Sequential Circuit Analysis and Design Flow -Registers and Counters	關國裕
	2009/1/8	Synchronous Sequential Logic -Latches and Flip-Flops -Synchronous Sequential Circuit Analysis and Design Flow -Registers and Counters	關國裕
	2009/1/15	Team Project or Final Exam	關國裕

七、評量方式**(Evaluation)** Participation: 10% Team Project: 30% Mid-term Exam: 30% Final Exam: 30%

八、講義位址**(http://)**

九、教育目標

重新查詢

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