十一、研究計畫中英文摘要：請就本計畫要點作一概述，並依本計畫性質自訂關鍵詞。

（二）計畫英文摘要。（五百字以內）

This project is to develop the frameworks for jointly designing the transmitter and receiver with block delay detection for block transmission systems with channel state information. The receivers using linear and nonlinear intrablock decision feedback equalization are investigated. For a single antenna or multiple antennas communication system, in the literature the block-based transmitter-receiver pair is jointly designed for a given channel matrix, which is usually assumed flat-fading or *equivalent* flat-fading (i.e., translated from a frequency-selective fading channel by inserting sufficient redundancy between blocks). Recently, a cascaded equalizing scheme, based on the oblique projection, is proposed by us to devise a minimum bit-error-rate(BER) block-based precoder with zero-forcing (ZF) equalization. The merit of the proposed framework is that it enables the joint design of a block-based precoder and the linear receiver for block transmissions with insufficient redundancy. In this project, a complete method for jointly designing the transceiver is pursued when the system block delay is considered being a design variable. The project is divided into two-year terms and the goal for each year is described as follows.

In the *first* year, a novel framework is developed for jointly designing a linear transmitter and a linear receiver. In such a framework, an optimum block-based precoder and a cascaded equalizer with optimum block delay detection are devised such that the average BER is minimized, subject to the transmission power constraint. The algorithms of determining the optimum block delay of the cascaded equalizer for minimizing BER are built for intrablock ZF and minimum mean square error (MMSE) equalization, respectively. In the *second* year, a nonlinear receiver is considered in the joint design of the transceiver. Particularly, a novel intrablock decision feedback equalizer (IDFE) is devised by applying the proposed cascaded equalizing structure with block delay in the feedforward equalizing path. Consequently, we design an optimum block-based precoder and an intrablock decision feedback equalizer with optimum block delay detection such that the average BER is minimized, subject to the transmission power constraint. The algorithms of determining the optimum block delay of the proposed IDFE for minimizing BER are also developed for intrablock ZF and MMSE equalization, respectively. Contrary to previous studies, the cases of using sufficient and insufficient redundancy for block transmissions are addressed in this project for the joint design of the transceiver.

Key words: block transmissions, precoder, redundancy, block delay detection, joint design, transceiver, intrablock decision feedback equalizer